Problem 2
Design and Implementation of a MIPS CPU with Multicycle Datapath
DATAPATH

1. INTRODUCTION

In this problem, you will design a custom RISC processor which is basically a stripped down MIPS processor. The goal of this problem is to provide you with a more practical hands-on approach to computer architecture design problems. The processor you will be designing is a 32-bit version of the MIPS processor; however, the instruction set will be a small subset of the actual MIPS ISA. You should implement the multicycle datapath version of the processor utilizing the VHDL hardware descriptive language. You may use any constructs within the VHDL language.

The processor supports the three instruction formats: R-format, I-format, and J-format as described in the text book and lectures. Table I Summarizes the core set of instructions for your ISA. The memory is assumed to be word addressable and each word is 32 bits.

Table I: Core MIPS Instruction Set to be Designed (with example)

OpCode [31 : 26]	Function Field [5 : 0]	Instruction	Operation
100011	--	lw	lw $s3, 300($t2)
101011	--	sw	sw $t6, 400($s7)
000000	100000	add	add $s5, $t3, $t1
000100	--	bne	beq $s6, $t5, 200
		(Custom set)	

The total set you need to design is the core set as above + a custom set designated for you as follows.

BEQ, ORI

2. Implementation Details

Your goal is to get the instruction set implemented and tested. This problem 2 will focus on the implementation of the datapath without the control design. Once the datapath is assembled, write a test bench or simulation script to test each instruction (e.g., with the examples given in Table I). If you work with abstraction in mind by first testing each lower part completely, it will eliminate potential errors within your design later.

Datapath Components

ALU implementation can be done similar to the example described in the text book. You can start with a 1-bit ALU cell and construct a 32-bit ALU unit. Note that you may have to modify the existing 1-bit cell design to provide more functions due to extended ISA in your CPU design.

3. Report

You are required to turn in a report that describes the design along with the VHDL code. The report should be typed, well written, and well organized. The suggested contents of the report are as follows:

- An overview of your design
- Appropriate sections to convey your report
- A discussion on how you tried to optimize your design
- A discussion on any improvements or additional features made to your design
- A discussion on what does not work correctly in your design
- An overview block diagram of your design. In order to draw this appropriately, you will have to understand the multi cycle MIPS code and its operation
- A sample simulation of your design that is annotated to show its correct operation.